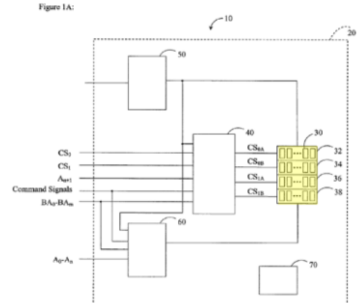
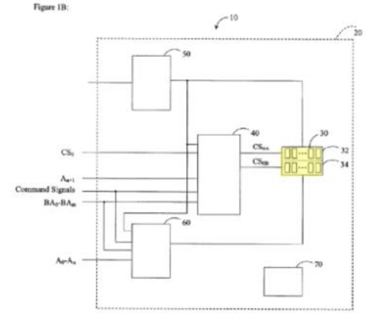
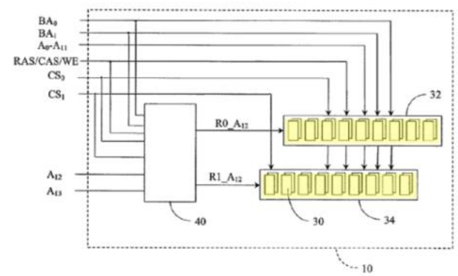
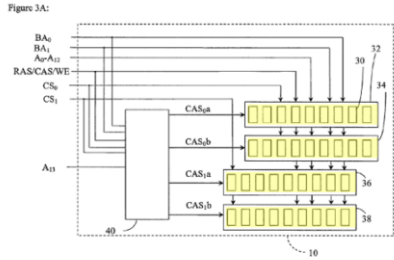
EXHIBIT A

CLAIM CONSTRUCTION POSITIONS AND SUPPORTING EVIDENCE

1. U.S. Patent No. 7,619,912

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"rank" (All claims)	"an independent set of DRAM devices on a memory module that act together to read or write the full, fixed bit-width of the memory module in response to command signals, including chip select signals, issued for one read or write transaction"	Support in Specification: • 12:13-25: "[I]n certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density . . ." • 7:9-13: "Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30." • 6:31-38: "[I]n certain embodiments, the memory devices 30 are arranged in four ranks, as schematically illustrated by FIG. 1A. In other embodiments, the memory devices 30 are arranged in two ranks, as schematically	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '912 and '417/'215 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the inventions. For example, the expert may testify as to the understanding by a POSITA of the term "rank." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. IPR2023-00203, EX2047, EX2105 through EX2108, EX2112, EX1034.

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		illustrated by FIG. 1B. Other numbers of ranks of the memory devices 30 are also compatible with embodiments described herein." • 7:55-8:43, 8:64-9:18: logic tables "for the selection among ranks of memory devices 30" • 10:31-35: "In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has, . . ." • Fig. 1A, 1B, 2A, 3A (showing multiple memory devices in each rank): Figure 1A: 	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		Figure 1B:  Figure 2A:  Figure 3A:  • 12:12-24: "In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. • Table 1 (7:56-8:10) (showing that the description that follows the logic diagram of Table 1 refers to ranks of multiple memory devices):	

<table>
<tr><th>Term, Phrase, or Clause</th><th>Netlist’s Proposed Construction</th><th>Exemplary Intrinsic Evidence</th><th>Exemplary Extrinsic Evidence</th></tr>
<tr><td></td><td></td><td>
Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.

TABLE 1
<table>
<tr><th>State</th><th>CS_0</th><th>CS_1</th><th>A_{n+1}</th><th>Command</th><th>CS_{0A}</th><th>CS_{0B}</th><th>CS_{1A}</th><th>CS_{1B}</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Active</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>1</td><td>Active</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>x</td><td>Active</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>1</td><td>0</td><td>0</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><th>State</th><th>CS_0</th><th>CS_1</th><th>A_{n+1}</th><th>Command</th><th>CS_{0A}</th><th>CS_{0B}</th><th>CS_{1A}</th><th>CS_{1B}</th></tr>
<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>Active</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>6</td><td>1</td><td>0</td><td>x</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>x</td><td>x</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. ‘x’ is a Don’t Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

act together to read or write:
8:46-60: “The ‘Command’ column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only . . . In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other
</td><td></td></tr>
</table>

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks . . . in such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time." • 2:16-18: "The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width." in response to a chip-select signal: • 2:34-38: "During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals." • Table 1 ($CS_0, CS_1,\ etc.$)	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		• 6:64-7:1: "In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged." <u>Prosecution History</u>: Prosecution History for Inter Partes Reexamination No. 95/000,578: Examiner allowed claim 16 by concluding that Amidi failed to teach "transmit[ting] a command signal to only one DDR memory device at a time when there is a plurality of memory devices in a rank." IPR2022-615, EX1010, at 3866. The Board affirmed this construction on appeal [Decision by PTAB in Inter Partes Reexamination Nos. 95/000,578; 95/000,579; and 95/001,339]: "Presumably, because Amidi discusses a particular cell within a bank, Requestor 1 contends that the command signals are being transmitted to one DDR memory device at a time as recited. Yet as the Examiner indicates:	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion . . . The claims require transmission of a command signal to only one DDR memory device at a time. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." IPR2022-615, EX1011, at 79.	

"A memory module connectable to a computer system, the memory module comprising" (All claims)	Preamble is limiting; and plain and ordinary meaning	Support in Specification: • 2:46-50: "In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board." • Abstract: "A memory module connectable to a computer system includes a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board." • 1:28-34: "These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, colunms, and banks which result in a total memory capacity for the memory module."	

		• 2:4-15: "The commercially-available 512-MB (64 Mx8-byte) memory modules and the 1-GB (128 Mx8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "x8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "x4" configurations are typically used in computer systems such as servers which are not as graphics-intensive." • 3:3-14: "In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a plurality of memory devices arranged in a first number of ranks. The memory module comprises means for coupling the memory module to the computer system. The memory module further comprises means for inputting a first set of control signals to the memory module. The first set	

		of control signals corresponds to a second number of ranks smaller than the first number of ranks. The memory module further comprises means for generating a second set of control signals in response to the first set of control signals." • 3:15-28: "In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a first memory device having a first data signal line and a first data strobe signal line. The memory module further comprises a second memory device having a second data signal line and a second data strobe signal line. The memory module further comprises a common data signal line connectable to the computer system. The memory module further comprises an isolation device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line. The isolation device selectively alternates between electrically coupling the first data signal line to the	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		common data signal line and electrically coupling the second data signal line to the common data signal line."	
"signal" (All claims)	Plain and ordinary meaning	Support in Specification: • 2:34-38: "During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals." • 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices."	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '912 and '417/'215 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the inventions. For example, the expert may testify as to the understanding by a POSITA of the term "signal." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. Wiley Electrical and Electronics Engineering Dictionary (1st ed. 2004) at 707.

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		• 5:36-41: "The register 60 receives and buffers a plurality of control signals, including address signals (e.g., bank address signals, row address signals, column address signals), and transmits corresponding signals to the appropriate memory devices 30." • 6:54-63: ". . . the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip select signals) and command signals from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." • 6:64-7:2: "In certain embodiments, the set of output control signals corresponds to a first number of ranks in	Newton's Telecom Dictionary (21st ed. 2005) at 761. McGraw-Hill Dictionary of Scientific and Technical Terms (6th ed. 2003) at 1929. Dictionary of Science and Technology (1st ed. 2003) at 555. Collins English Dictionary (7th ed. 2005) at 1499. The New Oxford American Dictionary (2nd ed. 2005) at 1578. Collins Dictionary Electronics Definitions for the Digital Age (2nd ed. 2004) at 378. ASTM Dictionary of Engineering Science & Technology (10th ed. 2005) at 557.

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." • 7:39-43: ". . . the memory module 10 receives row/column address signals or signal bits . . . bank address signals . . . chip-select signals . . . and command signals (e.g., refresh, precharge, etc.) from the computer system." • 7:46-49: "The logic element 40 receives the two chip-select signals (CS_0, CS_1) and one row/column address signal . . . from the computer system. • Table 1, 7:55-8:19:	

<table>
<tr><th>Term, Phrase, or Clause</th><th>Netlist's Proposed Construction</th><th>Exemplary Intrinsic Evidence</th><th>Exemplary Extrinsic Evidence</th></tr>
<tr><td></td><td></td><td>
Logic Tables
Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.
TABLE 1
<table>
<tr><th>State</th><th>CS_0</th><th>CS_1</th><th>A_{n+1}</th><th>Command</th><th>CS_{0A}</th><th>CS_{0B}</th><th>CS_{1A}</th><th>CS_{1B}</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Active</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>1</td><td>Active</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>x</td><td>Active</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>1</td><td>0</td><td>0</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>State</td><td>CS_0</td><td>CS_1</td><td>A_{n+1}</td><td>Command</td><td>CS_{0A}</td><td>CS_{0B}</td><td>CS_{1A}</td><td>CS_{1B}</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>Active</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>6</td><td>1</td><td>0</td><td>x</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>x</td><td>x</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
8:19-43: "In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0. In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1. In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks O and 1. In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting
</td><td></td></tr>
</table>

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		Rank 2. In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3. In Logic State 6: CS_1 is active low, A_{n+1}, is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3. In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high." • 21:28-33: "In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module 10 comprising pairs of the 512-Mb 128 M×4 memory devices 30 supplies the address and control signals including the extra row address (A13) to the memory module 10."	

"row[/column] address signal" (All claims)	Plain and ordinary meaning	Support in Specification: • 7:39-46: The memory module 10 receives row/column address signals or signal bits 40 ($A_0 - A_{n+1}$), bank address signals ($BA_0 - BA_m$), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The $A_0 - A_n$ row/column address signals are received by the register 60, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices 30." • 7:56-59: "The logic element 40 receives the two chip-select signals ($CS_0, CS_1,$ $etc.$) and one row/column address signal . . . from the computer system. • Table 1, 7:55-8:19:	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '912 and '417/'215 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term "row/column address signal." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses.

Logic Tables

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

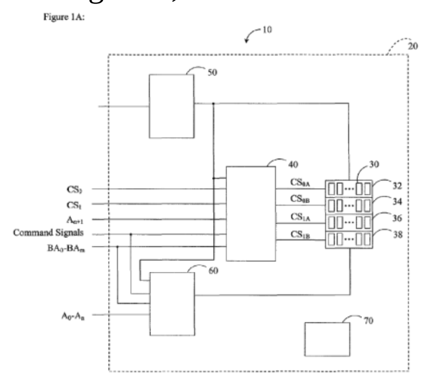
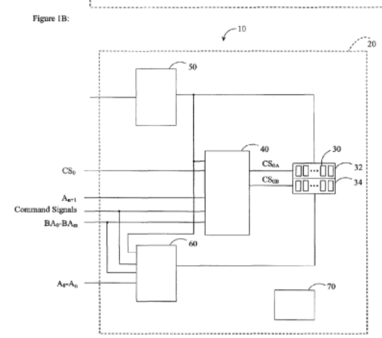
TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

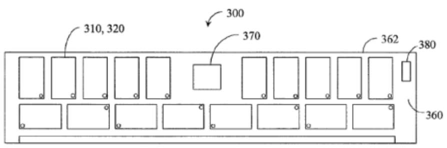
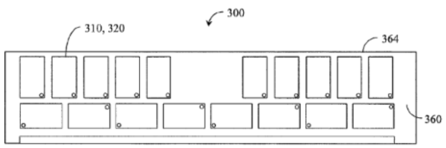
- 8:19-43: "In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0. In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1. In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks O and 1. In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2. In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B}

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		is pulled low, thereby selecting Rank 3. In Logic State 6: CS_1 is active low, A_{n+1}, is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3. In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high." • $A_0 - A_n$ in Figs. 1A, 1B.	
"coupled to the printed circuit board" (Claims 15, 16, 28, 86, 88)	Plain and ordinary meaning	Support in Specification: • 2:46-50: "The memory module comprises a printed circuit board, a plurality of memory devices coupled to the printed circuit board, and a logic element coupled to the printed circuit board." • 5:9-25: "The memory module 10 comprises a printed circuit board 20 and a plurality of memory devices 30 coupled to the printed circuit board 20 . . . The memory module 10 further comprises a logic element 10 coupled to the printed board 20 . . . [T]he memory module 10 further	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '912 and '417/'215 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the inventions. For example, the expert may testify as to the understanding by a POSITA of the term "coupled to [a] printed circuit board." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		comprises a phase-lock loop device 50 coupled to the printed circuit board 20 and a register 60 coupled to the printed circuit board 20." • Figs. 1A, 1B:   a plurality of double-data-rate (DDR) memory devices "coupled to the printed circuit board." • 5:9-12: "The memory module 10 comprises a printed circuit	testimony of Defendants' expert(s) and witnesses. Wiley Electrical and Electronics Engineering Dictionary (1st ed. 2004) at 151. Newton's Telecom Dictionary (21st ed. 2005) at 219. McGraw-Hill Dictionary of Scientific and Technical Terms (6^{th} ed. 2003) at 501. Dictionary of Science and Technology (1st ed. 2003) at 151. Collins Dictionary Electronics Definitions for the Digital Age (2nd ed. 2004) at 95. Merriam-Webster's Collegiate Dictionary (11th ed. 2008) at 286. Cambridge Dictionary of American English (2nd ed. 2008) at 191. Longman Dictionary of American English (4th ed. 2008) at 232.

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		board 20 and a plurality of memory devices 30 coupled to the printed circuit board 20." • 5:11-13: "The memory module further comprises a logic element 40 coupled to the printed circuit board 20." • 5:23-25: "the memory module 10 further comprises . . . a register 60 coupled to the printed circuit board 20." • 5:23-24: "the memory module 10 further comprises a phase-lock loop device 50 coupled to the printed circuit board 20."	The American Heritage Dictionary of the English Language (4th ed. 2006) at 419. Macmillan English Dictionary for Advanced Learners (2nd ed. 2007) at 338. The New Oxford American Dictionary (3rd ed. 2005) at 397.

"mounted to the printed circuit board" (Claims 1, 39, 77, 80, 82, 90)	Plain and ordinary meaning	Support in Specification: • 1:26-31: "Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system." • 6:12-16: "Memory devices 30 compatible with embodiments described herein include, but are not limited to, random access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR-1, DDR-2, DDR-3)." • Figs. 11A, 11B:	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '912 patent were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term "mounted to [a] printed circuit board." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. Wiley Electrical and Electronics Engineering Dictionary (1st ed. 2004) at 484. McGraw-Hill Dictionary of Scientific and Technical Terms (6th ed. 2003) at 1377. Dictionary of Science and Technology (1st ed. 2003) at 406. Collins English Dictionary (7th ed. 2005) at 1064.

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		Figure 11A:  Figure 11B:  • 5:25-27: "In certain embodiments, the phase-lock loop device 50 and the register 60 are each mounted on the printed circuit board." • Figs. 1A, 1B.	

"wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output [control] signals ***in response*** at least in part ***to*** (i) the [at least one] row address signal, (ii) the bank address signals, and (iii) the [at least one] chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal" (Claims 1, 15, 28, 39)	Plain and ordinary meaning	Support in Specification: • 5:18-20: "The logic element 40 generates a set of output control signals in response to the set of input control signals." • 6:54-63: ". . . the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip select signals) and command signals from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." "wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals" • Figs. 1A, 1B, 3A, 3B; • 17:28-19:52 [Verilog code] • 22:50-63: "To access the additional memory density of the high-density memory module 10, the two chip-select signals (CS0 , CS 1) are used	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '912 and '417/'215 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the inventions. For example, the expert may testify as to the understanding by a POSITA of the term "respond to," being "responsive to," and "in response to." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. Wiley Electrical and Electronics Engineering Dictionary (1st ed. 2004) at 659. McGraw-Hill Dictionary of Scientific and Technical Terms (6th ed. 2003) at 1797. Dictionary of Science and Technology (1st ed. 2003) at 522.

		with other address and control signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 Mx8-byte DDR-1 DRAM memory module, the CS0 and CS 1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 3A. FIG. 3B schematically illustrates an exemplary logic element 40 compatible with embodiments described herein. In certain embodiments, the logic element 40 comprises a programmable-logic device (PLD) 42 and four "OR" logic elements 52, 54, 56, 58 electrically coupled to corresponding ranks 32, 34, 36, 38 of memory devices 30." • 23:6-25: "In the embodiment schematically illustrated by FIG. 3B, the PLD 42 transmits each of the four "enabled CAS" (ENCAS0 a, ENCAS0b, ENCAS1a, ENCAS1b) signals to a corresponding one of the "OR" logic elements 52, 54,	ASTM Dictionary of Engineering Science & Technology (10th ed. 2005) at 514. The American Heritage Dictionary of the English Language (4th ed. 2006) at 1486. Bloomsbury English Dictionary (2nd ed. 2004) at 1589. Longman Business English Dictionary (2nd ed. 2007) at 462.

		56, 58. The CAS signal is also transmitted to each of the four "OR" logic elements 52, 54, 56, 58. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements 52, 54, 56, 58, the PLD 42 is able to select which of the four ranks 32, 34, 36, 38 is active. In certain embodiments, the PLD 42 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 32, 34, 36, 38. In certain other embodiments, the PLD 42 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, andCS1b) which are each transmitted to a corresponding one of the four ranks 32, 34, 36, 38." "of the output [control] signals ***in response***"	

		• 6:55-63: "As schematically illustrated by FIGS. IA and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." "(i) the [at least one] row address signal," • A_{n+1} in Figs. 1A, 1B; • $A13$ in Figs. 3A, 3B; • 7:46-53: "The logic element 40 receives the two chip-select signals (CS0 , CS1) and one row/column address signal (An+i) from the computer system. Both the logic element 40 and the register 60 receive the bank address signals (BA0-BAm) and at least one	

		command signal (e.g., refresh, precharge, etc.) from the computer system." "(ii) the bank address signals," • $BA_0 - BA_m$ in Figs. 1A, 1B; • BA_0, BA_1 in Figs. 3A, 3B; • 7:46-53: "The logic element 40 receives the two chip-select signals (CS0 , CS1) and one row/column address signal (An+i) from the computer system. Both the logic element 40 and the register 60 receive the bank address signals (BA0-BAm) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system." "and (iii) the [at least one] chip-select signal of the [set/plurality] of input [control] signals" • CS_0, CS_1 in Fig. 1A; • CS_0 in Fig. 1B; • 7:46-53: "The logic element 40 receives the two chip-select signals (CS0 , CS1) and one row/column address signal (An+i) from the computer system. Both the logic element 40 and the register 60 receive the bank address signals (BA0-	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		BAm) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system." "and (iv) the PLL clock signal" • Figs. 1A, 1B; • 5:29-30: "In response to signals received from the computer system, the phase-lock loop device 50 transmits clock signals to the plurality of memory devices 30, the logic elements 40, and the register 60." • 17:28-19:52 [Verilog code] - "clk_in"	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"wherein the logic element ***responds to*** at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks" (Claim 77)	Plain and ordinary meaning	*See* intrinsic evidence for "in response … to."	*See* evidence for "in response … to."

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"wherein the generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element ***responsive*** at least in part ***to*** (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device" (Claim 80)	Plain and ordinary meaning	*See* intrinsic evidence for "in response … to."	*See* evidence for "in response … to." Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '912 patent were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term "based on." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. *See also* Merriam-Webster's Collegiate Dictionary (11th ed. 2008) at 101.

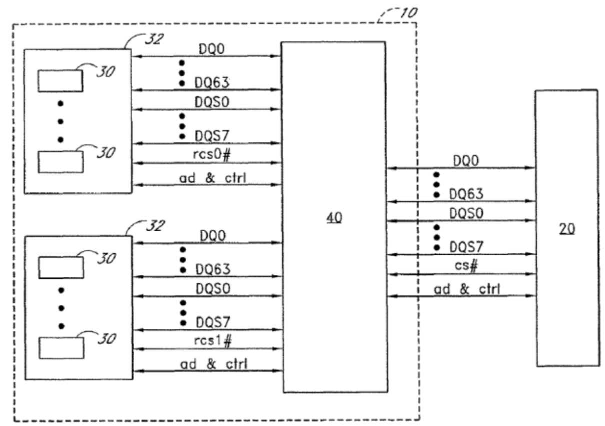
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
			Cambridge Dictionary of American English (2nd ed. 2008) at 62. Longman Dictionary of American English (4th ed. 2008) at 75. The American Heritage Dictionary of the English Language (4th ed. 2006) at 148. Macmillan English Dictionary for Advanced Learners (2nd ed. 2007) at 107. The New Oxford American Dictionary (3rd ed. 2005) at 136.

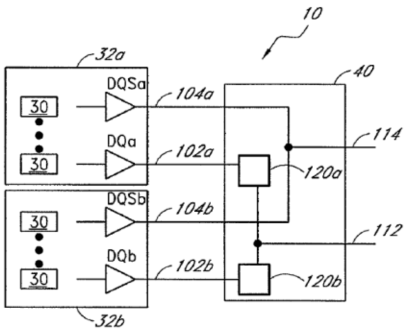
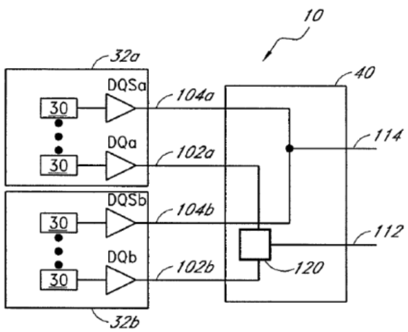
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"wherein the logic element ***responds to*** at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input [control] signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output [control] signals that is greater than double or equal to double the number of chip-select signals of the set of input [control] signals" (Claim 82, 86)	Plain and ordinary meaning	*See* intrinsic evidence for "in response … to."	*See* evidence for "in response … to."
"wherein the logic element ***responds to*** at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set	Plain and ordinary meaning	*See* intrinsic evidence for "in response … to."	*See* evidence for "in response … to."

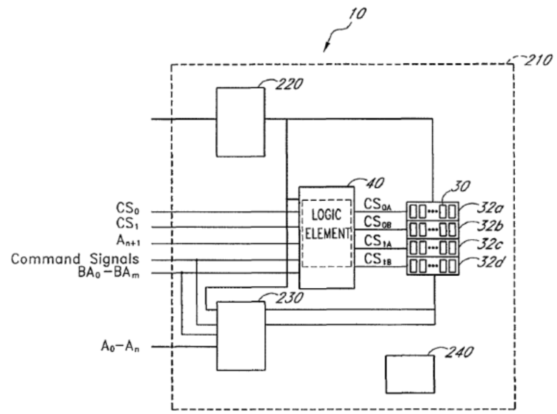
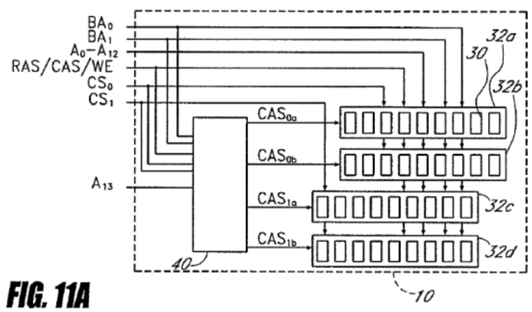
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals" (Claim 88)			
"wherein the logic element ***responds to*** at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals" (Claim 90)	Plain and ordinary meaning	*See* intrinsic evidence for "in response … to."	*See* evidence for "in response … to."

2. U.S. Patent No. 9,858,215

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"rank" (All claims)	*See* "rank" (912 patent)	'215, 2:41-52 ("The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization. The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.") '215, FIGS 1, 4A-4B, 5C-5D, 8A-9B, 10A, 11A and accompanying descriptions (depicting ranks 32a/b/c/d with memory devices 30):	*See* "rank" (912 patent)

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		 FIG. 1	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		 FIG. 4A  FIG. 4B	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		FIG. 9A FIG. 11A '215 Prosecution History: 283: Amendment based on PTAB interview adding the language: "A memory module operable in a computer system to communicate data with a memory controller of the computer system via a data bus"	

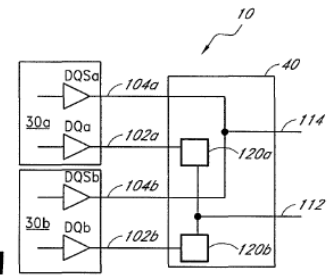
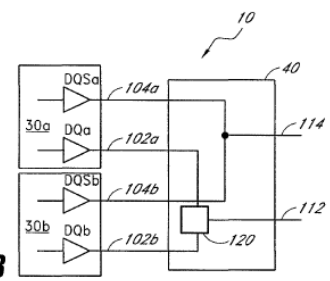
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"operable in a computer system to communicate data" (Claim 1)	Plain and ordinary meaning	'215 at Abstract ("A memory module is operable to communicate data with a memory controller via a memory bus in response to memory commands received from the memory controller.") '215, 3:11-28 ("In certain embodiments, a memory module is operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller. . . .In certain embodiments, the printed circuit board has a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. The register is configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command.") '215, 3:57-61 ("The second control signals are different from the first control signals, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller.")	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '215/'417 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term "operable in a computer system to communicate data." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses.

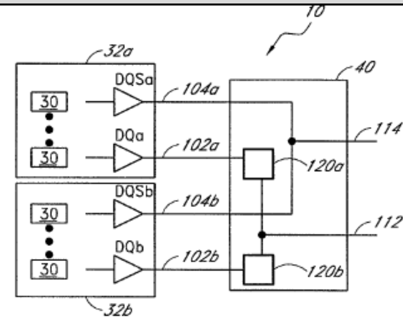
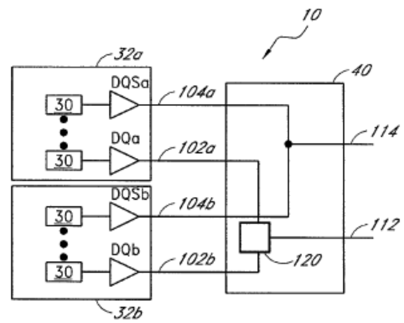
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		’215, cl. 1 (“1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising: a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; . . .”) ’215 Prosecution History: 283-284 : Amendment based on PTAB interview adding language to claim 1: a plurality of memory integrated circuits <u>mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits</u> including at least one first memory integrated circuit <u>in the first rank</u> and at least one second memory integrated circuit <u>in the second rank,</u>	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		<u>wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the</u> <u>first memory command</u>; and"	
"logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"; (Claim 1)	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	Abstract ("… The memory module further comprises logic providing first control signals to the buffer to enable communication of a first data burst between the memory controller and the at least one first memory integrated circuit through the buffer in response to a first memory command ….") 3:11-56 ("The memory module comprises a printed circuit board, a register coupled to the printed circuit board, a plurality of memory integrated circuits mounted on the printed circuit board, a buffer, and logic coupled to the buffer…In certain embodiments, the buffer is coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus. The logic	*See* evidence for "coupled to" and "respond to"/"in response ... to." Dictionary Definition for Logic: McGraw-Hill Dictionary of Scientific and Technical Terms (5th ed. 1994) Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications

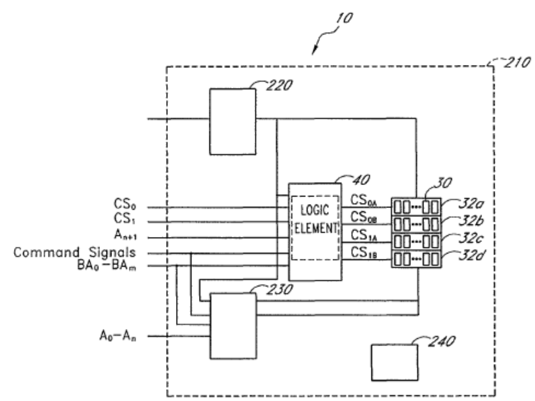
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		is configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory 50 integrated circuit and the memory controller through the buffer. The logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer." 6:37-59 ("In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable- logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable- logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in	leading to the '215/'417 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term "respond to," "coupled," "burst" and "data burst." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. Simon Collin, Dictionary of Science and Technology (2nd ed. 2007) at 91.

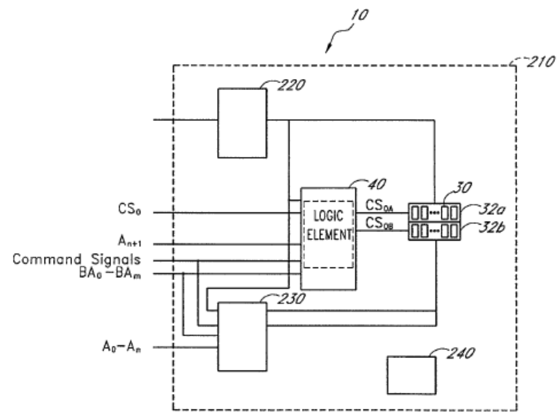
Term, Phrase, or Clause	**Netlist's Proposed Construction**	**Exemplary Intrinsic Evidence**	**Exemplary Extrinsic Evidence**
		certain 50 other embodiments, the logic element comprises one or more integrated circuits. In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.")	Dictionary of Computer and Internet Terms, Vol. 1 (2016) at 75. Wiley Electrical and Electronics Engineering Dictionary at 85. Bruce L. Jacob, Synchronous DRAM Architectures, Organizations, and Alternative Technologies (2002) at 10. Hewlett-Packard, Memory Technology Evolution: An Overview of System Memory Technologies (2008) at 5. IEEE 100 The Authoritative Dictionary of IEEE Standards Terms (7th ed. 2000) at 127, 128.

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		 FIG. 3A  FIG. 3B	

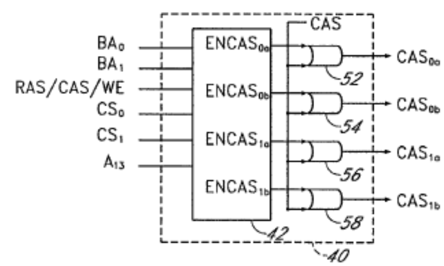
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		FIG. 4A  FIG. 4B  8:57-9:17 ("In the example embodiments schematically illustrated by FIGS. **3A, 3B, 4A,** and **4B,** the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		operatively coupled to the switches **120,** as schematically illustrated by FIGS. **5A-5D.** The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays FPGA), custom-designed semiconductor devices, and complex programmable- logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.") 9:65-11:36 ("An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		six FET switches for providing load isolation to DQ and DQS lines… [Table of Code]") 13:21-26 ("While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40,** in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40,** as schematically illustrated by FIG. **8D.**")  **FIG. 9A**	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		 ***FIG. 9B*** Figs. 9A and 9B; 15:21-56 ("As schematically illustrated by FIGS. **9A** and **9B**, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals. . . In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		module **10** is larger than the number of memory devices **30** per memory module for 50 which the computer system is configured to utilize. ***In certain embodiments, the circuit 40 comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10.***" 16:4-17:40 (logic tables) 22:58-23:16 ("The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10.** In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples **1** and **2** provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples **1** and 2 includes logic to reduce potential problems due to "back-to-back	

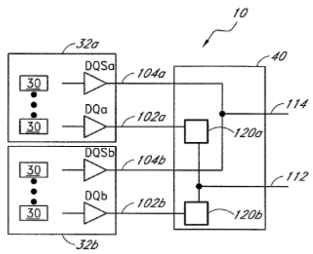
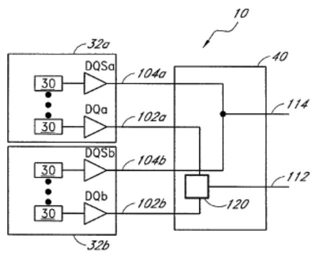
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein. An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to **1** Gb using DDR2 memory devices with the BA2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which 15 generates two chip-select signals.") 23:20-26:60 (Verilog code)  FIG. 11B 29:27-30:4 ("FIG. **11B** schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain	

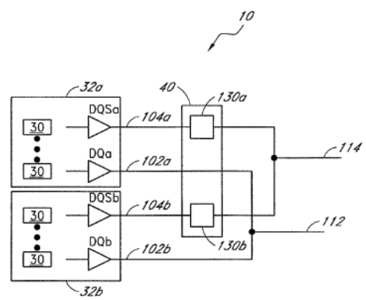
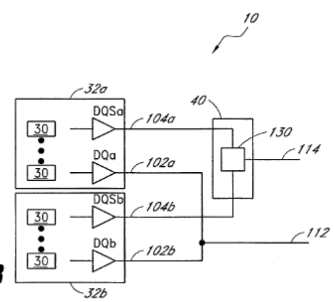
Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		embodiments, the circuit **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52, 54, 56, 58** electrically coupled to corresponding ranks **32a, 32b, 32** ***c*****, 32** *d* of memory devices **30.** In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52, 54, 56, 58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52, 54, 56, 58** in accordance with embodiments described herein. In the embodiment schematically illustrated by FIG. **11B,** the PLD **42** transmits each of the four "enabled CAS "(ENCAS0 a, ENCAS0b, ENCAS1a, ENCAS1b) signals to a corresponding one of the "OR" logic elements **52, 54, 56, 58.** The CAS signal is also transmitted to each of the four "OR" logic elements **52, 54, 56, 58.** The CAS signal and the"enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52, 54, 56, 58,** the PLD **42** is able to select which of the four ranks **32a, 32b, 32** ***c*****, 32** *d* is active…")	

Term, Phrase, or Clause	**Netlist's Proposed Construction**	**Exemplary Intrinsic Evidence**	**Exemplary Extrinsic Evidence**
		<u>**From '215 Prosecution History**</u> Pg. 130: a buffer coupled between the at least one first memory integrated circuit and the data bus, and between the at least one second memory integrated circuit and the data bus~~, wherein the buffer is configured in response to the first memory command to provide a first data path between the at least one first memory integrated circuit and the data bus while the memory module is receiving or outputting the first data burst in response to the first memory command, and wherein the buffer is configured in response to the second memory command to provide a second data path between the at least one second memory integrated circuit and the data bus while the memory module is receiving or outputting the second data burst in response to the second memory command, the second data path being different from the first data path~~<u>, and</u> <u>logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between</u>	
"wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals" (Claim 1)	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	*See above* Abstract (…"The memory module further comprises logic providing first control signals to the buffer to enable communication of a first data burst between the memory controller and the at least one first memory integrated circuit through the buffer in response to a first memory command, and providing second control signals to the buffer to enable communication of a second data burst between the at least one second memory integrated circuit and the memory bus through the buffer in response to a second memory command.") 3:44-61 ("…The logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst	*See* evidence for "coupled to" and "respond to"/"in response ... to." *See* evidence for "logic coupled to" above.

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		between the at least one second memory integrated circuit and the memory controller through the buffer. The second control signals are different from the first control signals, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller.")	
"in response to the first memory command, providing first control signal to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"; and (Claim 21)	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	**From '215 patent Specification:** 3:44-61 ("In certain embodiments, the buffer is coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus. The logic is configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer. The logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer. The second control signals are different from the first control	*See* evidence for "in response to"

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		signals, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller. 6:24-36 ("In certain embodiments, the plurality of memory devices 30 comprises a first number of memory devices 30. In certain such embodiments, the circuit 40 selectively isolates a second number of the memory devices 30 from the computer system, with the second number less than the first number. In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks. For example, in certain embodiments, the memory devices 30 are arranged in two ranks, as schematically illustrated by FIG. 1. In other embodiments, the memory devices 30 are arranged in four ranks. Other numbers of ranks of the memory devices 30 are also compatible with embodiments described herein."	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		 FIG. 4A  FIG. 4B 8:12-56 ("… The memory modules 10 of FIGS. 4A and 4B comprises two ranks 32a, 32b, with each rank 32a, 32b having a corresponding set of DQ data signal lines and a corresponding set Of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices 30 of the memory module 10 are also compatible with certain embodiments described herein. For simplicity, FIGS. 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank 32. The circuit 40 of FIG. 4A selectively isolates one or more of the DQ data signal lines 102a, 102b of the two	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		ranks 32a, 32b from the computer system. Thus, the circuit 40 selectively allows a DQ data signal to be transmitted from the memory controller 20 of the computer system to the memory devices 30 of one or both of the ranks 32a, 32b via the DQ data signal lines 102a, 102b. In addition, the circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first rank 32a and a second DQ data signal from the DQ data signal line 102b of the second rank 32b to be transmitted to the memory controller 20 via the common DQ data signal line 11…")  FIG. 8A  FIG. 8B	

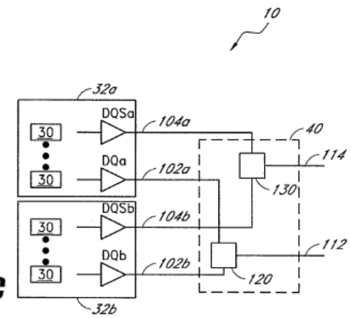
<table>
<tr><th>Term, Phrase, or Clause</th><th>Netlist's Proposed Construction</th><th>Exemplary Intrinsic Evidence</th><th>Exemplary Extrinsic Evidence</th></tr>
<tr><td></td><td></td><td>


FIG. 8C

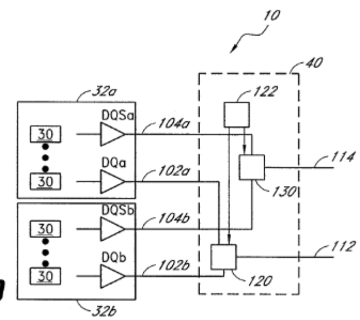


FIG. 8D

12:25-66 ("FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules 10 comprising a circuit 40 which multiplexes the DQS data strobe signal lines 104a, 104b of two ranks 32a, 32b from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines 104a, 104b of FIGS. SA-SD correspond to two ranks 32a, 32b of memory devices 30, in certain other embodiments, the circuit 40 multiplexes the DQS data strobe signal
</td><td></td></tr>
</table>

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		lines 104a, 104b corresponding to two individual memory devices.") 13:1-49 ("In certain embodiments, as schematically illustrated by FIG. 8B, the circuit 40 comprises a switch 130 which multiplexes the DQS data strobe signal lines 104a, 104b from one another. For example, the circuit 40 receives a DQS data strobe signal from the common DQS data strobe signal line 114 and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line 104a, to the second DQS data strobe signal line 104b, or to both DQS data strobe signal lines 104a, 104b. As another example, the circuit 40 receives a first DQS data strobe signal from the first rank 32a of memory devices 30 and a second DQS data strobe signal from a second rank 32b of memory devices 30 and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line 114. . .The circuit 40 of certain embodiments controls the isolation of the DQS data strobe signal lines 104a, 104b by monitoring commands received by the memory module 10 from the computer system and producing "windows" of operation whereby the appropriate switches 130 are activated or deactivated to enable and disable the DQS data	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		strobe signal lines 104a, 104b to mitigate BARX collisions. In certain other embodiments, the circuit 40 monitors the commands received by the memory module 10 from the computer system and selectively activates or deactivates the switches 120 to enable and disable the DQ data signal lines 102a, 102b to reduce the load of the memory module 10 on the computer system. In still other embodiments, the circuit 40 performs both of these functions together.") 32:55-67 ("In certain embodiments, the memory module 400 comprises a plurality of memory devices configured in pairs, each pair having a first memory device 410 and a second memory device 420. For example, in certain embodiments, a 128 Mx72-bit DDR SDRAM high-density memory module400 comprises thirty-six 64 Mx4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device 410 of each pair has the first DQS pin 412 electrically coupled to the second DQS pin 422 of the second memory device 420 of the pair. In addition, the first DQS pin 412 and the second DQS pin 422 are concurrently active when the first memory device 410 and the second memory device 420 are concurrently enabled.") **From '215 Patent Prosecution History:**	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		133: in response to the first memory command, providing ~~a first data path~~ first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer ~~data bus while the memory module is receiving or outputting the first data burst in response to the first memory command~~; and in response to the second memory command, providing ~~a second data path~~ second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals ~~data bus while the memory module is receiving or outputting the second data burst in response to the second memory command, the second data path being different from the first data path~~.	
"in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals" (Claim 21)	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	*See above*	*See* evidence for "burst" above. *See* evidence for "in response … to."
"the memory module has an overall ***CAS latency***" / "overall	Plain and ordinary meaning	"In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS	Netlist may rely on expert testimony to explain the technology,

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
CAS latency of the memory module" (Claims 3, 4, 24, 25)		latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array.. . The one-cycle time delay of certain such embodiments provides sufficient time ***for read and write data transfers*** to provide the functions of the data path multiplexer/demultiplexer." 16:22-17:13:	the state of the art at the time the applications leading to the '215/'417 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term "CAS latency," "overall CAS latency of the memory module," and "actual operational CAS latency" of an SDRAM device. Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. Wiley Electrical and Electronics Engineering

<table>
<tr><th>Term, Phrase, or Clause</th><th>Netlist's Proposed Construction</th><th>Exemplary Intrinsic Evidence</th><th>Exemplary Extrinsic Evidence</th></tr>
<tr><td></td><td></td><td>
TABLE 1
<table>
<tr><th>State</th><th>CS_0</th><th>CS_1</th><th>A_{n+1}</th><th>Command</th><th>CS_{0A}</th><th>CS_{0B}</th><th>CS_{1A}</th><th>CS_{1B}</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Active</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>1</td><td>Active</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>x</td><td>Active</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>1</td><td>0</td><td>0</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>Active</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>6</td><td>1</td><td>0</td><td>x</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>x</td><td>x</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note:
1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. "x" is a Don't Care condition.
4. Command involves 2 number of command signals that define operations such as refresh, precharge, and other operations.

In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.
In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.
In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.
In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.
In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_1B is pulled low, thereby selecting Rank 3.
In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_1B are pulled low, thereby selecting Ranks 2 and 3.
In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

"The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh."

17:13-35:
</td><td>Dictionary (2004) at 532.

High Definition, An A to Z Guide to Personal Technology (2006) at 49.

Micron DDR4 SDRAM Datasheet, EDY4016A, (2014) at 39.

Bruce L. Jacob, Synchronous DRAM Architectures, Organizations, and Alternative Technologies (2002) at 10.

Hewlett-Packard, Memory technology evolution: an overview of system memory technologies (2008) at 3, 4.

JEDEC Terms, Definitions, and Letter Symbols for Microcomputers,</td></tr>
</table>

<table>
<tr><th>Term, Phrase, or Clause</th><th>Netlist’s Proposed Construction</th><th>Exemplary Intrinsic Evidence</th><th>Exemplary Extrinsic Evidence</th></tr>
<tr><td></td><td></td><td>
Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using gated CAS signals.

TABLE 2
<table>
<tr><th>CS*</th><th>RAS*</th><th>CAS*</th><th>WE*</th><th>Density Bit</th><th>A₁₀</th><th>Command</th><th>CAS0*</th><th>CAS1*</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>NOP</td><td>x</td><td>x</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>x</td><td>x</td><td>NOP</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>x</td><td>ACTIVATE</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>x</td><td>ACTIVATE</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>x</td><td>READ</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>x</td><td>READ</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>x</td><td>WRITE</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>x</td><td>WRITE</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>PRE-CHARGE</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>PRE-CHARGE</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>x</td><td>1</td><td>PRE-CHARGE</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>x</td><td>x</td><td>MODE REG SET</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>x</td><td>x</td><td>REFRESH</td><td>0</td><td>0</td></tr>
</table>

23:10-25:32 (Verilog Code Example 2)

25:34-24:60 (Verilog Code Example 3)

30:16-18 (“The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data.”)

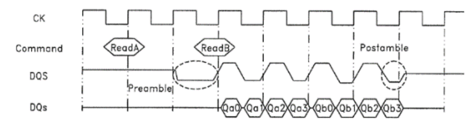
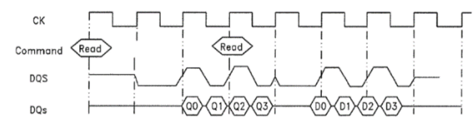
7:46-52 “While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would
</td><td>
Microprocessors, and Memory Integrated Circuits, JESD100B.01 (2002) at 2, 11.

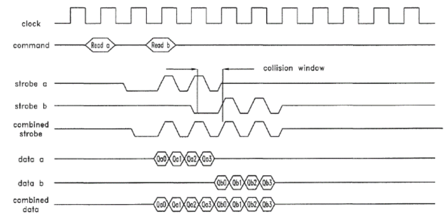
JESD79-2A at 24
</td></tr>
</table>

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		be denoted by triangles on the DQ or DQS lines pointing away from the memory controller)." 20:22-47 ("In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40.** The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20.** The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer").	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"actual operational CAS latency of each of the plurality of memory integrated circuits" / "actual operational CAS latency of the memory integrated circuits" (Claims 3, 4, 24, 25)	Plain and ordinary meaning	*See above*	*See* evidence for "CAS latency" above.
"burst of data strobe signals" (Claims 12, 13, 28, 29)	Plain and ordinary meaning	*See* '215 patent at 11:38-57 ("Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read	*See* evidence for "burst" above. *See* also JESD79 (IPR2023-00455, EX1060). JESD79-2 (IPR2023-00455, EX1064).

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. **FIG. 6A** shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device."); *id.* 11:58-12:4 ("In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of **FIG. 6B** for successive read accesses from different memory devices."). *See* Fig. 6A, 6B; '215 patent 4:17-24 ("**FIG. 6A** shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device. **FIG. 6B** shows an exemplary timing diagram with an extra clock cycle between successive read commands	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		issued to different memory devices for successive read accesses from different memory devices.**)**  ***FIG. 6A***  ***FIG. 6B*** *See also* '215 patent 12:13-24 ("In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in **FIG. 7**, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window.") *See also* '215 patent Fig. 7:	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		 FIG. 7 *See* '215 patent at 12:25-13:15 (**FIGS. 8A-8D** schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104** a , **104** b of two ranks **32** a , **32** b from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104** a , **104** b of **FIGS. 8A-8D** correspond to two ranks **32** a , **32** b of memory devices **30** , in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104** a , **104** b corresponding to two individual memory devices **30** a , **30** b. **FIG. 8A** schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104** a , **104** b from one	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		another during the transition from the first read data burst of one rank **32** a of memory devices **30** to the second read data burst of another rank **32** b of memory devices **30.** In certain embodiments, as schematically illustrated by **FIG. 8A**, the circuit **40** comprises a first switch **130** a electrically coupled to a first DQS data strobe signal line **104** a of a first rank **32** a of memory devices **30** and a second switch **130** b electrically coupled to a second DQS data strobe signal line **104** b of a second rank **32** b of memory devices **30**. In certain embodiments, the time for switching the first switch **130** a and the second switch **130** b is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32** a and before the first DQS data strobe of the read data burst of the second rank **32** b). During the read data burst for the first rank **32** a, the first switch **130** a is enabled. After the last DQS data strobe of the first rank **32** a and before the first DQS data strobe of the second rank **32** b, the first switch **130** a is disabled and the second switch **130** b is enabled. As shown in **FIG. 8A**, each of the ranks **32** a , **32** b otherwise involved in a BBARX collision have their DQS data strobe signal lines **104** a , **104** b selectively electrically coupled to the common	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		DQS line **114** through the circuit **40** . The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104** a , **104** b of the two ranks **32** a , **32** b of memory devices **30** from one another to avoid a BBARX collision. In certain embodiments, as schematically illustrated by **FIG. 8B**, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104** a, **104** b from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104** a , to the second DQS data strobe signal line **104** b , or to both DQS data strobe signal lines **104** a , **104** b . As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32** a of memory devices **30** and a second DQS data strobe signal from a second rank **32** b of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114)** *See* '215 patent at 6:60-7:13; Figure 2 ("**FIG. 2** schematically illustrates a circuit diagram of two memory devices **30** a , **30** b of a conventional memory module showing the interconnections between the DQ data signal lines **102** a , **102** b of the memory devices **30** a , **30** b and the DQS data	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		strobe signal lines **104** a , **104** b of the memory devices **30** a , **30** b . Each of the memory devices **30** a , **30** b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, **FIG. 2** only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30** a , **30** b . The DQ data signal lines **102** a , **102** b and the DQS data strobe signal lines **104** a , **104** b are typically conductive traces etched on the printed circuit board of the memory module. As shown in **FIG. 2**, each of the memory devices **30** a , **30** b has their DQ data signal lines **102** a , **102** b electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104** a , **104** b electrically coupled to a common DQS line **114** . The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30** a , **30** b concurrently.") *See* '215 patent at 3:11-61; 4:35-59 *See* '215 patent at 30:16-23 ("The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). *See also* IPR2022-00745, Paper 19 at 27, 39 (indicating "Two bursts of two strobe signals"); id. at 41 ("Claim 22,8 which depends on claim 15, recites that "the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank and the memory controller at a specified data rate." Ex. 1001, Claim 22 (emphasis added). For N-bit wide data signals and data strobes to be transferred between the first N-bit wide rank and the memory controller in the context of claim 22, the data signals and strobes must be transferred (1) into and out of the first N-bit wide rank, (2) through the circuitry (Limitation [15.9]), and (3) out of and in to the memory module to and from the memory controller. Ex. 2003, ¶63. And according to claim 22, that transfer must occur at a single, specified data rate. Id. This is generally shown below as applied to Fig. 4A of the '314 Patent, wherein "a specified data rate" has been assigned a value of 1 for illustrative purposes. "). *See generally* evidence for "burst" above	

Term, Phrase, or Clause	**Netlist's Proposed Construction**	**Exemplary Intrinsic Evidence**	**Exemplary Extrinsic Evidence**
"the at least one of the circuit components" (Claim 15)	Plain and ordinary meaning	*See* Claim 14 (which claim 15 is dependent on) ("14. The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller."); Claim 1 ("a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus"). *See also* '215 patent at **3:44-61** ("In certain embodiments, the buffer is coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus. The logic is configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer. The logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer.	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		The second control signals are different from the first control signals, a circuit is configured to be mounted on a memory module that is operable to communicate data with a memory controller via a data bus in response to memory commands received from the memory controller.") *See also* '215 patent at **14:37-60** (**[0074]** In certain embodiments, as schematically illustrated in **FIG. 9A**, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit **40**, and the register **230. The register 230 receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices 30. In certain embodiments, the register 230 comprises a plurality of register devices. While the phase-lock loop device 220, the register 230, and the circuit 40**	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device 220, the register 230, and the circuit 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein) *See also* '215 patent at **14:61-15:3 ([0075]** In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210** . These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.) *See also* '215 patent at **20:22-47** ("In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. **This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines.** In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time."). *See also* '215 patent at **5:18-32 ("FIG. 1** schematically illustrates an example memory module **10** compatible with certain embodiments	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10.")** *See also* '215 patent at **6:29-59 ([0046]** In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg.,	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits. **[0047]** In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.").***See also* '215 patent at 7:53-8:10; 8:38-56 ("[0051]** For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** a, **120** b on the DQ data signal lines **102** a, **102** b as schematically illustrated by **FIG. 3A**. Each switch **120** a , **120** b is selectively actuated to selectively electrically couple the DQ data signal line **102** a to the common DQ signal line **112** , the DQ data signal line **102** b to the common DQ signal line **112** , or both DQ data signal lines **102** a , **102** b to the common DQ signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102** a, **102** b, as	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		schematically illustrated by **FIG. 3B**. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102** a to the common DQ signal line **112** , the DQ data signal line **102** b to the common DQ signal line **112** , or both DQ signal lines **102** a , **102** b to the common DQ signal line **112** . Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30** a , **30** b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, FIGS. **3** A and **3** B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30** a , **30** b for simplicity. The configurations schematically illustrated by **FIGS. 3A and 3B** can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**."). ***See also*** **'215 patent at 8:57-9:17 ([0054]** In the example embodiments schematically illustrated by **FIGS. 3A, 3B, 4A, and 4B**, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by **FIGS. 5A-5D**. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.) *See also* '215 patent at **9:18-43** ("In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g.,	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10** , including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.").	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		See also '215 patent at **12:44-59 ([0066]** In certain embodiments, as schematically illustrated by **FIG. 8A**, the circuit **40** comprises a first switch **130** a electrically coupled to a first DQS data strobe signal line **104** a of a first rank **32** a of memory devices **30** and a second switch **130** b electrically coupled to a second DQS data strobe signal line **104** b of a second rank **32** b of memory devices **30**. In certain embodiments, the time for switching the first switch **130** a and the second switch **130** b is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32** a and before the first DQS data strobe of the read data burst of the second rank **32** b). During the read data burst for the first rank **32** a, the first switch **130** a is enabled. After the last DQS data strobe of the first rank **32** a and before the first DQS data strobe of the second rank **32** b, the first switch **130** a is disabled and the second switch **130** b is enabled.) *See also* '215 patent at **13:16-35 ([0069]** In certain embodiments, the circuit **40** also provides the load isolation described above in reference to **FIGS. 1-5**. For example, as schematically illustrated by **FIG. 8C**, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102** a , **102** b and the switch **130** for the DQS data strobe signal lines **104** a , **104** b . While in certain	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		embodiments, the switches **130** are integral with a logic element of the circuit **40** , in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40** , as schematically illustrated by **FIG. 8D**. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10** . Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex.) *See also* '215 patent at **15:30-56 ([0079]** In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		example, in the exemplary embodiment as schematically illustrated by **FIG. 9A**, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of **FIG. 9B**, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30** . In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. **In certain embodiments, the circuit 40 comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10)** *See also* '215 patent at **28:9-26 ([0147] FIG. 10B** schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by **FIG. 10B**, **the circuit 40 comprises a programmable-logic device (PLD) 42, a first multiplexer 44 electrically coupled to the first rank 32 a of memory devices 30 , and a second multiplexer 46 electrically coupled to the second rank 32 b of memory devices 30**. **In certain embodiments, the PLD 42 and the first and second multiplexers 44, 46 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42 , first multiplexer 44 , and second multiplexer 46 in accordance with embodiments described herein.)** *See also* '215 patent at **29:27-30:3** (**[0153]** To access the additional memory density of the high-density memory module **10** , the two chip-select signals (CS0, CS1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS0 and CS1 **signals** along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		FIG. 11A. **FIG. 11B** schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40** comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32** a, **32** b, **32** c, **32** d of memory devices **30**. **[0154]** In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic **elements 52** , **54** , **56** , **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54** , **56** , **58** in accordance with embodiments described herein **[0155]** In the embodiment schematically illustrated by **FIG. 11B**, the PLD **42** transmits each of the four "enabled CAS" (ENCAS0 a, ENCAS0 b, ENCAS1 a, ENCAS1 b) signals to a corresponding one of the "OR" logic elements **52** , **54** , **56** , **58** . The CAS signal is also transmitted to each of the four "OR" logic elements **52** , **54** , **56** , **58** . The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52** , **54** , **56** , **58** , the PLD **42** is able to	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		select which of the four ranks **32** a , **32** b , **32** c , **32** d is active. **[0156]** In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks **32** a , **32** b , **32** c , **32** d . In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0 a, CS0 b, CS1 a, and CS1 b) which are each transmitted to a corresponding one of the four ranks **32** a, **32** b, **32** c , **32** d.) *See also* Fig. 3A, 3B, 4A, 4B, 5A-5D, 8A, 8B, **9A, 9B, 10B; 11A-B;** *See also* IPR2023-00455 paper 1 (petition) at 80 ("Furthermore, a POSITA would have understood that, because interfaces 520a/b, 510, and 590 include transceivers (e.g., 575), and because multiplexer/ demultiplexer circuit 597 (e.g., in 591) contains "multiplexing logic and demultiplexing logic," Perego's buffer device includes logic that sends "control signals" to the transceivers, multiplexing/ demultiplexing circuits, and to the input and output latches to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write operations."	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		EX1003, ¶¶318-319; EX1071, 14:62-15:6 ("The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction."), 17:41-44 ("The multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations"), 17:61-62, Figs.5A-5B.); IPR2023-00455 paper 1 (petition) at 107-110 ("Ground 1 teaches, as explained above for [1.d.2]-[1.d.3], [1.e.], [1.f.1]-[1.f.2] (pp.63-80), "*[t]he memory module of claim 1, wherein the buffer includes circuit components* [e.g., in multiplexers 530a and 530b, and interfaces 520a, 520b and 510 or 590 (and respective transceivers in those interfaces), shown below] *configurable to provide a first data path* [e.g., to interface 520a for the channel 370 to the first rank, green, below] *or a second data path* [e.g., to interface 520b for the channel 370 to the second rank, blue, below] *depending on whether the first rank or the second rank is selected to communicate data with the memory controller*." EX1003, ¶¶483-488); ("Ground 1 teaches, as explained above for [1.d.2]-[1.d.3], [1.e.], [1.f.1]-[1.f.2] (pp.63-80), "*[t]he memory module of claim 14, the*[5] *at least one of the circuit components* [from claim 14 (pp.107-109)] *is configured to provide the first data path* [from claim 14 (pp.107-109)] *in response to the first control signals* [from [1.f.1] (pp.76-80)], *and is*	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		configured to provide the second data path [from claim 14 (pp.107-109)] *in response to the second control signals* [from [1.f.2] (pp.76-80)]." EX1003, ¶¶489-494.).	

3. U.S. Patent No. 11,093,417

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"rank" (All claims)	*See* the same term for the '912 and '215 patents		

See '417, 2:47-58 ("The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.")

'417, FIGS 1, 4A-4B, 5C-5D, 8A-9B, 10A, 11A and accompanying descriptions (depicting ranks 32a/b/c/d with memory devices 30):

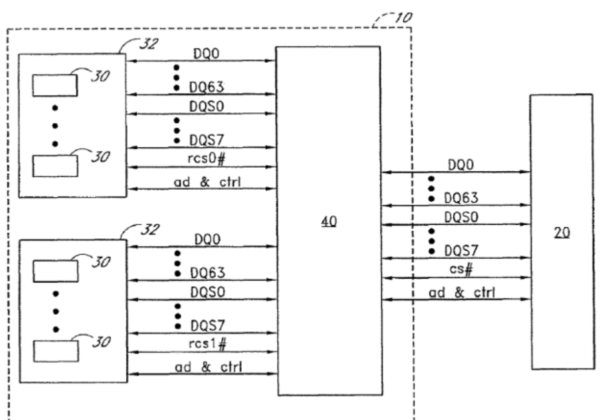


FIG. 1

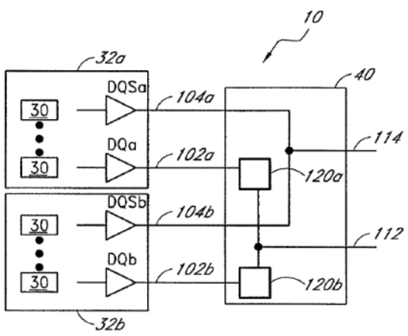

10
32a
40
DQSa
104a
30
30
DQa
102a
114
120a
30
DQSb
104b
112
30
DQb
102b
120b
32b

FIG. 4A

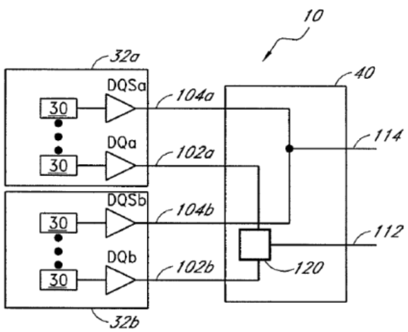

10
32a
40
DQSa
104a
30
DQa
102a
114
30
30
DQSb
104b
112
30
DQb
102b
120
32b

FIG. 4B

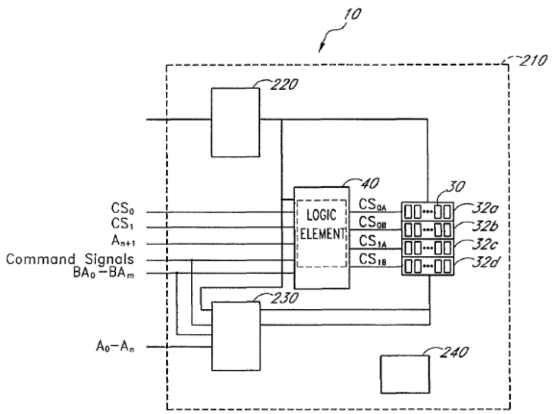


FIG. 9A

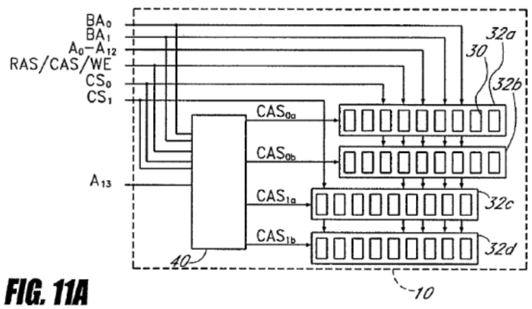


FIG. 11A

	***See* the same term for the ’912 patent.**		
“operable in a computer system to communicate data” (Claim 1)	Plain and ordinary meaning	’417 at Abstract (“A memory module operable to communicate data with a memory controller via a N-bit wide memory bus comprises memory devices arranged in a plurality of N-bit wide ranks.”)	*See* the same term in the ’215 patent.

		'417 at 3:18-28 ("A memory module is operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller. The memory bus includes address and control signal lines and data signal lines. According to some embodiments, the memory module comprises a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and memory devices mounted on the printed circuit board.") '417, cl. 1 ("A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising: a printed circuit board having a plurality of edge	

		connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; . . .”)	
“data buffer control signals” (Claims 1, 3, 11)	Plain and ordinary meaning	’417 at Abstract (“The memory module further comprises logic configurable to receive a set of input address and control signals associated with a read or write memory command and output registered address and control signals and data buffer control signals. . . . The circuitry is configurable to enable registered transfers of N-bit wide data signals associated with the memory read or write command between the N-bit wide memory bus and the memory devices in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices.”) ’417, 3:50-52 (“The logic is further configurable to output data buffer control signals in response to the read or write memory command.”) ’417, 4:1-6(“The circuitry is configurable to transfer the burst of	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the ’215/’417 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding

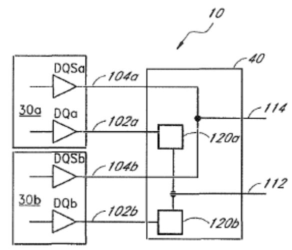
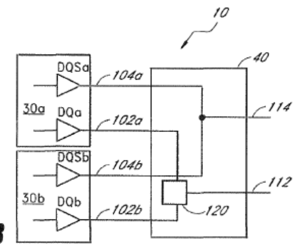
		N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module.") '417, 4:23-29 ("In some embodiments, the circuitry includes data paths, and the circuitry is configured to enable the data paths in response to the data buffer control signals so that the N-bit wide data signals are transferred via the data paths. In some embodiments, the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.") '417, 7:32-35 ("In certain embodiments, the circuit 40 further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element.") '417, 9:37-50 ("In the example embodiments schematically illustrated by FIGS. 3A, 3B, 4A, and 4B, the circuit 40 comprises a logic element which is integral with and	by a POSITA of the term "signal" and "data buffer control signals." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses. See also extrinsic evidence for "signal."

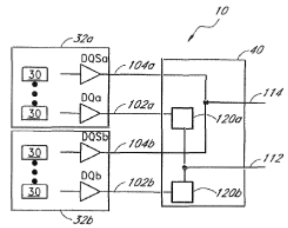
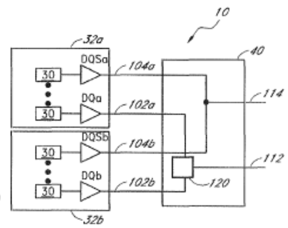
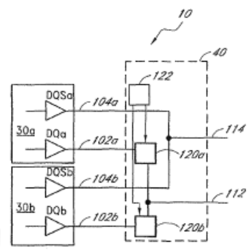
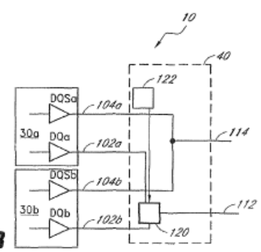
		comprises the switches 120 which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch 120 comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit 40 comprises a logic element 122 which is a separate component operatively coupled to the switches 120, as schematically illustrated by FIGS. 5A-5D. The one or more switches 120 are operatively coupled to the logic element 122 to receive control signals from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line.") *See also, e.g.*: '417, 4:56-60 ("FIGS. **4A and 4B** schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.")	

		’417, 5:16-18 (“FIG. **9B** schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.”) ’417, 7:10-13 (“In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by FIG. 1.”) ’417, 8:65-9:9 (“The memory modules **10** of FIGS. 4A and 4B comprises two ranks **32** *a*, **32** *b*, with each rank **32** *a*, **32** *b* having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. . . . The circuit **40** of FIG. 4A selectively isolates one or more of the DQ data signal lines **102** *a*, **102** *b* of the two ranks **32** *a*, **32** *b* from the computer system.”) ’417, 10:5-11 (“In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load	

		(e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled.”) 14:37-46 (“FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104** *a*, **104** *b* of two ranks **32** *a*, **32** *b* from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104** *a*, **104** *b* of FIGS. 8A-8D correspond to two ranks **32** *a*, **32** *b* of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104** *a*, **104** *b* corresponding to two individual memory devices **30** *a*, **30** *b.”*)	
“circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide	Plain and ordinary meaning, that is, the limitation does not require the first rank and second rank of memory integrated circuits to be on different forks and the term is not a 112(b) term.	*See* evidence for “data buffer control signals” above. ’417, 3:644:6 (“In some embodiments, the memory module further comprises circuitry coupled between the data signal lines in the N-bit wide memory bus and	*See* extrinsic evidence for “burst” and “in response ... to.”

memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal" (Claim 1)		corresponding data pins of memory devices in each of the plurality of N-bit wide ranks. The circuitry is configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module.") '417, 4:23-45 ("In some embodiments, the circuitry includes data paths, and the circuitry is configured to enable the data paths in response to the data buffer control signals so that the N-bit wide data signals are transferred via the data paths. In some embodiments, the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry. In some embodiments, the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the	

		respective series of write data bits are successively transferred via a respective one of the data paths.”) Figs 3A-5D and accompanying descriptions, e.g.,  FIG. 3A  FIG. 3B	

		 FIG. 4A  FIG. 4B  FIG. 5A  FIG. 5B *E.g.*, ’417, 8:10-10:4 (“As schematically illustrated by FIGS. 3A and 3B, an example memory	

		module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102** *a*, **102** *b* of the two memory devices **30** *a*, **30** *b* from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102** *a*, **102** *b*. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102** *a* of the first memory device **30** *a* or a second DQ data signal from the DQ data signal line **102** *b* of the second memory device **30** *b* to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see, e.g., triangles on the DQ and DQS lines of FIGS. 3A and 3B which point towards the memory controller). **. . .** In the example embodiments schematically illustrated by FIGS. 3A, 3B, 4A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal	

		lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by FIGS. 5A-5D. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic	

		devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.") **<u>417 Prosecution History</u>** Pg. 29- Reasons for Allowance: "Claim I recites the limitation, 'the circuitry being configurable to transfer the burst of Nbit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.' Said limitations are taught by the specification as originally filed. Said limitations, in combination with the other recited limitations, are not taught or suggested by the prior art of record… Janzen (US 2003/0018845)	

		appears to be the closest prior art and teaches a memory device having a number of ranks having different burst order addressing for read and write operations. However, does not teach the limitation, 'the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.'"	
"circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry" (Claim 6)	Plain and ordinary meaning	*See* evidence for term immediately above. *See also, e.g.,* '417, 22:49-51 ("The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines.")	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the

			’215/’417 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term “circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus

			through the circuitry." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses.
"circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths" (Claim 11)	Plain and ordinary meaning, not a 112(6) term	*See* evidence for preceding two claim terms.	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '215/'417 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim

			element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term "enable [] data paths in response to [] data buffer control signals" and "burst of … data signals." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses.

			See also evidence for "burst."
"logic . . . configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, . . . the logic is further configurable to output data buffer control signals in response to the read or write memory command" (Claim 1)	Plain and ordinary meaning, not a 112(6) term	*See, e.g.*, '417 at Abstract ("The memory module further comprises logic configurable to receive a set of input address and control signals associated with a read or write memory command and output registered address and control signals and data buffer control signals. . . . The circuitry is configurable to enable registered transfers of N-bit wide data signals associated with the memory read or write command between the N-bit wide memory bus and the memory devices in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices.") '417, 3:50-52 ("The logic is further configurable to output data buffer control signals in response to the read or write memory command.") '417, 4:1-6("The circuitry is configurable to transfer the burst of N-bit wide data signals between the	*See* evidence for "in response ... to." *See* evidence for "logic"

		N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module.”) ’417, 4:23-29 (“In some embodiments, the circuitry includes data paths, and the circuitry is configured to enable the data paths in response to the data buffer control signals so that the N-bit wide data signals are transferred via the data paths. In some embodiments, the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.”) ’417, 7:32-35 (“In certain embodiments, the circuit 40 further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element.”) ’417, 9:37-50 (“In the example embodiments schematically illustrated by FIGS. 3A, 3B, 4A, and 4B, the circuit 40 comprises a logic element which is integral with and comprises the switches 120 which	

		are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch 120 comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit 40 comprises a logic element 122 which is a separate component operatively coupled to the switches 120, as schematically illustrated by FIGS. 5A-5D. The one or more switches 120 are operatively coupled to the logic element 122 to receive control signals from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line.") IPR2023-00454, Paper 6 ("The memory module 10 also includes a circuit 40 electrically coupled to the memory devices 30 and to the memory controller 20 of the computer system. *Id.*, 6:4-7. The circuit 40 includes a logic that translates between a system memory domain of the computer system and a physical memory domain of the memory module 10. *Id.*, 6:9-12. This may be achieved by the logic receiving input data signals, chip-select signals and other	

		control/address signals from the memory controller 20, and outputting corresponding registered data signals, registered chip select signals and other registered control/address signals to the memory devices 30.")	
"the read or write command" (Claims 1, 15)	Plain and ordinary meaning	'417, 3:58-63 ("One of the plurality of ranks receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command.") '417, 4:29-35 ("In some embodiments, the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths.")	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '215/'417 patents were filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may

			testify as to the understanding by a POSITA of the term "read or write command." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses.
"the predetermined amount of time delay" (Claim 9)	Plain and ordinary meaning	'415, 4:1-15 ("The circuitry is configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module. In some embodiments, data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module	Netlist may rely on expert testimony to explain the technology, the state of the art at the time the applications leading to the '215/'417 patents were filed, the level of ordinary skill in the

		is greater than an actual operational CAS latency of each of the memory devices. In some embodiments, the memory module further comprises a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, and the predetermined amount of time delay is at least one clock cycle time delay.") '417, 22:41-61 ("In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which	relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. For example, the expert may testify as to the understanding by a POSITA of the term a "predetermined amount of time delay." Netlist may also rely on the expert to respond to Defendants' claim construction positions and any testimony of Defendants' expert(s) and witnesses.

		is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.”)	
“overall CAS latency of the memory module” (Claim 1)	Plain and ordinary meaning	’417 at Abstract (“The circuitry is configurable to enable registered transfers of N-bit wide data signals associated with the memory read or write command between the N-bit wide memory bus and the memory devices in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices.”) ’417, 4:1-10 (“The circuitry is configurable to transfer the burst of	*See* extrinsic evidence for “CAS latency.”

		N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module. In some embodiments, data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.") '417, 22:36-61 ("In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an	

		incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.") '417, 26:16-29:20 (Verilog code example 2, including code to "determine the cas latency")	

		<u>417 Prosecution History</u> Pg. 29- Reasons for Allowance: "Claim I recites the limitation, 'the circuitry being configurable to transfer the burst of Nbit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.' Said limitations are taught by the specification as originally filed. Said limitations, in combination with the other recited limitations, are not taught or suggested by the prior art of record… Janzen (US 2003/0018845) appears to be the closest prior art and teaches a memory device having a number of ranks having different burst order addressing for read and write operations. However, does not teach the limitation, 'the circuitry being configurable to transfer the	

		burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an additional amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.'"	
"actual operational CAS latency of each of the memory devices" (Claim 1)	Plain and ordinary meaning	*See* above intrinsic evidence for "overall CAS latency of the memory module."	*See* extrinsic evidence for "CAS latency."
"wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices" (Claim 1)	Plain and ordinary meaning	*See* above intrinsic evidence for "overall CAS latency of the memory module."	*See* extrinsic evidence for "CAS latency" and "an amount of time delay."

4. U.S. Patent No. 10,268,608

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
"A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising" (Claim 1)	Preamble is limiting; and plain and ordinary meaning	*See* Claim 1 element 2 ("a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal"); element 3 (". . . the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines"); element 4 ("a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		respective set of memory devices . . . .”). *See* description 3:25-50 (“A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device,	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines."). *See* 4:20-35 ("FIG. 1 shows a system 100 including a memory controller (MCH) 101 and one or more memory modules 110 coupled to the MCH by a memory bus 105 , according to one embodiment. As shown, the memory bus includes C/A signal lines 120 and groups of system data/strobe signal lines 130. Also as shown, each memory module 110 has a plurality of memory devices 112 organized in a plurality of ranks 114. Each memory module 110 further includes a module control circuit (module controller or module control device) 116 coupled to the MCH 101 via the C/A signal lines 120 , and a plurality of buffer circuits	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		or isolation devices 118 coupled to the MCH 101 via respective groups of system data/strobe signal lines 130 . In one embodiment, the memory devices 112 , the module control circuit 116 and the isolation devices 118 can be mounted on a same side or different sides of a printed circuit board (module board) 119.”). *See* 4: 36-45 (“In the context of the present description, a rank refers to a set of memory devices that are selectable by a same chip select signal from the memory controller. The number of ranks of memory devices in a memory module 110 may vary. For example, as shown, each memory module 110 may include four ranks of memory devices 112 . In another embodiment, the memory module 110 may include 2 ranks of memory devices. In yet another embodiment, the memory module may include six or more ranks of memory devices 112.”). *See* 4:65-5:57 (“Referring to FIG. 2A, which illustrates one memory module 110 according to an embodiment, the module control device 116 receives	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		system memory commands represented by a set of system control/address (C/A) signals from the MCH 101 via signal lines 120 and generates module command signals and module control signals based on memory commands from the system. The module control device 116 also received a system clock MCK and generates a module clock signal CK in response to the system clock signal MCK. The MCK signal may include a pair of complementary clock signals, MCK and MCK , and the module clock signal may include a pair of complementary clock signals CK and CK. Examples of the system C/A signals include, but are not limited to, Chip Select (or /CS) signal, which is used to select a rank of memory devices to be accessed during a memory (read or write) operation; Row Address Strobe (or /RAS) signal, which is used mostly to latch a row address and to initiate a memory cycle; Column Address Strove (or /CAS) signal, which is used mostly to latch a column address and to initiate a read or write operation; address signals, including bank address signals and row/column address signals,	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		which are used to select a memory location on a memory device or chip; Write Enable (or /WE) signal, which is used to specify a read operation or a write operation, Output Enable (or /OE) signal, which is used to prevent data from appearing at the output until needed during a read operation, and the system clock signal MCK. Examples of module command signals include, but are not limited to module /CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		embodiments, the module command signals may also include the module clock signal CK. Examples of module control signals include, but are not limited to a mode signal (MODE), which specifies a mode of operation (e.g., test mode or operating mode) for the isolation devices 118; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals. In one embodiment, the module control signals are transmitted to the isolation devices 118 via respective module control signal lines 230. Alternatively, the module control signals can be packetized before being transmitted to the isolation devices 118 via the module control signal lines and decoded/processed at the isolation devices.”). *See* 9:10-10 (“In one embodiment, each data buffer 118 has a set of configurable operations, including, for example: programmable phase	

Term, Phrase, or Clause	Netlist's Proposed Construction	Exemplary Intrinsic Evidence	Exemplary Extrinsic Evidence
		relationship between the clock it receives and the clock it regenerates, programmable phase adjustment for the data and data-strobe signals coupled to the memory devices 112, programmable phase adjustment for the data and data-strobe signals coupled to the system memory controller 101, programmable phase adjustment related to at least one control signal that is coupled to the control circuit 116.") *See also* Fig. 1, 2A, 2B	